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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,477	01/28/2004	Leonard Forbes	M4065.0381/P381-A	9433

24998 7590 08/11/2006

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Washington, DC 20006-5403

EXAMINER
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THOMAS, TONIAE M

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/765,477	FORBES ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 September 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 68-91 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 89 is/are allowed.
- 6) ☒ Claim(s) 68,69,90 and 91 is/are rejected.
- 7) ☒ Claim(s) 70-88 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. This Office action is a response to the amendment filed on 27 September 2005.
2. Currently, claims 68-91 are pending

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 68, 69, 90, and 91 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (US 6,097,070).<sup>1</sup>

### **Regarding claims 68 and 69**

The Mandelman et al. patent (Mandelman) discloses a method of forming a semiconductor transistor (figs. 2, 3A-3C and accompanying text). The method comprises: forming a first gate dielectric 27 over a substrate 20 (fig. 3A; col. 3, line 59; and col. 4, lines 10-11); forming a first type conductive gate

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<sup>1</sup> The Applicant submitted the Mandelman et al. patent as prior art (see PTO Form 1449 filed on 28 January 2004). The patent reference was also cited in the parent application, Serial No. 09/808,114.

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region 25 over the first gate dielectric (fig. 3B and col. 4, lines 12-15);<sup>2</sup> forming a dielectric layer 29 on the sides of the first type conductive layer (fig. 3C and col. 4, lines 19-29); forming a second gate dielectric 28 over the substrate (fig. 3C and col. 4, lines 19-29); forming a second type conductive gate region 26 over the second gate dielectric, adjacent to the dielectric layer, and on the sides of the first type conductive region (fig. 3C and col. 4, lines 35-39); and forming source and drain regions 21 in the substrate to define a channel region between them and beneath the first and second conductive type gate regions (fig. 2 ad col. 5, lines 1-5), wherein the first gate dielectric, first type conductive gate region, second gate dielectric, and second type conductive gate region are wholly between the source and drain regions.<sup>3</sup>

In one preferred embodiment, the first type conductive region is of P+ conductivity type and the second type conductive region is of N+ conductivity type (col. 4, lines 12-15 and col. 4, lines 36-50).

Regarding claims 90 and 91

Again, Mandelman discloses a method of forming a semiconductor transistor (figs. 2, 3A-3C and accompanying text). The method comprises: providing a substrate 20 (fig. 3A and col. 3, line 59); forming a first gate

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<sup>2</sup> In one preferred embodiment, the gate region 25 is a P+ type conductive gate (col. 4, lines 12-15). In this Office action, the P+ conductive type is designated as the first conductive type.

<sup>3</sup> Given the broadest, reasonable interpretation, the claim language "wholly between," as recited in claims 68 and 90, is interpreted to mean that the first gate dielectric, the first type conductive gate region, the second gate dielectric, and the second type conductive gate region are required to at least completely cover the portion of the substrate between the source and

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dielectric layer 27 over the substrate (fig. 3A and col. 4, lines 10-11); forming a first gate electrode 25 having sidewalls over the first gate dielectric layer (fig. 3B and col. 4, lines 12-15, wherein in one preferred embodiment the first gate electrode has a first work function (abstract, lines 11-13 and col. 4, lines 36-50); forming a dielectric layer 29 on the sidewalls of the first gate electrode (fig. 3C and col. 4, lines 19-29); forming a second gate dielectric 28 over the substrate (fig. 3C and col. 4, lines 19-29); forming a pair of second gate electrodes 26 over the second gate dielectric and adjacent to the dielectric layer, the second gate electrodes being separated from the first gate electrode by the dielectric layer (fig. 3C and col. 4, lines 35-39), wherein in one preferred embodiment the pair of second gate electrodes has a second work function which is different than the first work function (abstract, lines 11-13 and col. 4, lines 36-50); forming a conductive cap 23 over each of the gate electrodes (fig. 3C and col. 4, lines 54-56); forming insulating sidewalls 22 adjacent to the conductive cap and the gate electrodes (fig. 2 and col. 4, line 66 - col. 5, line 1), and forming source and drain regions 21 in the substrate to define a channel region between them and beneath the first and second conductive type gate regions (fig. 2 ad col. 5, lines 1-5), wherein the first gate dielectric, first type conductive gate region, second gate dielectric, and second type conductive gate region are wholly between the source and drain regions. <sup>4</sup>

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drain regions 21. However, the claim language does not preclude overlapping of the source and drain regions, as shown in fig. 2 of the Mandelman et al. patent reference.

<sup>4</sup> See Footnote No 3.

In one preferred embodiment, the second work function is more negative than the first work function (col. 4, lines 36-50).

***Allowable Subject Matter***

4. Claims 70-88 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. As explained in the previous Office action mailed on 16 June 2005, the prior art of record does not anticipate, teach or suggest a method of forming a semiconductor transistor substantially as claimed, wherein the method comprises forming the P+ type conductivity region, as recited in claim 70.

5. Claim 89 is allowable over the prior art of record. As explained in the previous action, Mandelman does anticipate teach or suggest the following limitations recited in claim 89: selectively etching the P+ type conductive layer to leave at least two substantially vertical P+ type conductive layer regions over the first gate dielectric; removing a portion of the first gate dielectric by selectively etching to the substrate, thereby leaving the vertical P+ type conductive layer regions over the remaining first gate dielectric; and etching the N+ type conductive layer to leave at least two structures, the two structures including the vertical P+ type conductive layer regions and the adjacent regions of the N+ type conductive layer. There is no teaching or

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suggestion within the prior art of record to modify Mandelman according to the claimed invention. Furthermore, while Mandelman discloses forming a dielectric layer 29 on the sidewalls of the P+ type conductive region 25, Mandelman does not anticipate, teach or suggest forming the dielectric layer of a nitride layer. There is no teaching or suggestion within the prior art of record to modify Mandelman by forming the dielectric layer of a nitride layer.

### ***Response to Arguments***

6. Applicant's arguments filed on 27 September 2005 have been fully considered but they are not persuasive.

7. In the reply filed on 27 September 2005, Applicants present the following argument:

The Mandelman et al. reference does not teach or suggest "forming source and drain regions in said substrate... wherein said first gate dielectric, first type conductive gate region, second gate dielectric, and second type conductive gate region are wholly between said source and drain regions."

As stated above, the claim language "wholly between," as recited in claims 68 and 90, is interpreted to mean that the first gate dielectric, the first type conductive gate region, the second gate dielectric, and the second type conductive gate region are required to at least completely cover that portion of the substrate between the source and drain regions 21. However, the claim language does not preclude an overlapping of the source and drain regions. While the first gate dielectric, the first type conductive gate region, the second gate dielectric, and the second type conductive gate region of Mandelman do indeed overlap the source and drain regions 21; the first gate dielectric, the

first type conductive gate region, the second gate dielectric, and the second type conductive gate region completely cover that portion of the substrate between the source and drain regions, as shown in fig. 2. Thus, the first gate dielectric, the first type conductive gate region, the second gate dielectric, and the second type conductive gate region are “wholly between” the source and drain regions.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

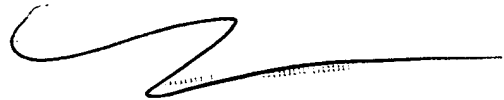
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TMT  
07 August 2006

A handwritten signature in black ink, appearing to read 'Mary Wilczewski', with a long horizontal line extending to the right.

**Mary Wilczewski**  
**Primary Examiner**